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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,982	09/17/2003	David Chong Sook Lim	112055-0040P1	4640

24267 7590 02/28/2007

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EXAMINER	
ANDUJAR, LEONARDO	
ART UNIT	**PAPER NUMBER**
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/664,982	LIM ET AL.	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5 and 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/10/2006 has been entered.

Election/Restrictions

2. Applicant's election without traverse of species 1 (fig. 3) in the reply filed on 03/24/2005 is acknowledged.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4, 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shim et al. (US 6,531,784) in view of Kang et al. (US 2003/017810 A1).

5. Regarding claim 1, Shim (e.g. figs. 9 & 5) shows a die containing package comprising: a die 14 defining electrical die contacts 34, the die contacts arranged along a first and an opposite side of the die (i.e. left side from the geometrical center line and right side from the geometrical center line of the chip), a substrate 30 defining first

substrate contacts 22, flattened electrical conductive balls 58 attached to the die contacts and making electrical connection thereto, electrical conductive runs 24 on the substrate that run substantially under the die connecting the first substrate contacts, wherein the first substrate contacts are located adjacent to the first side of the die, to second substrate contacts 22, wherein the second substrate contacts are located adjacent to the opposite side of the die, electrically conductive wires 28 with first ends making electrical connections to the first substrate contacts, wherein the wires are formed to run substantially parallel to the surface of the die, and wherein the other ends are horizontally attached to the flattened balls.

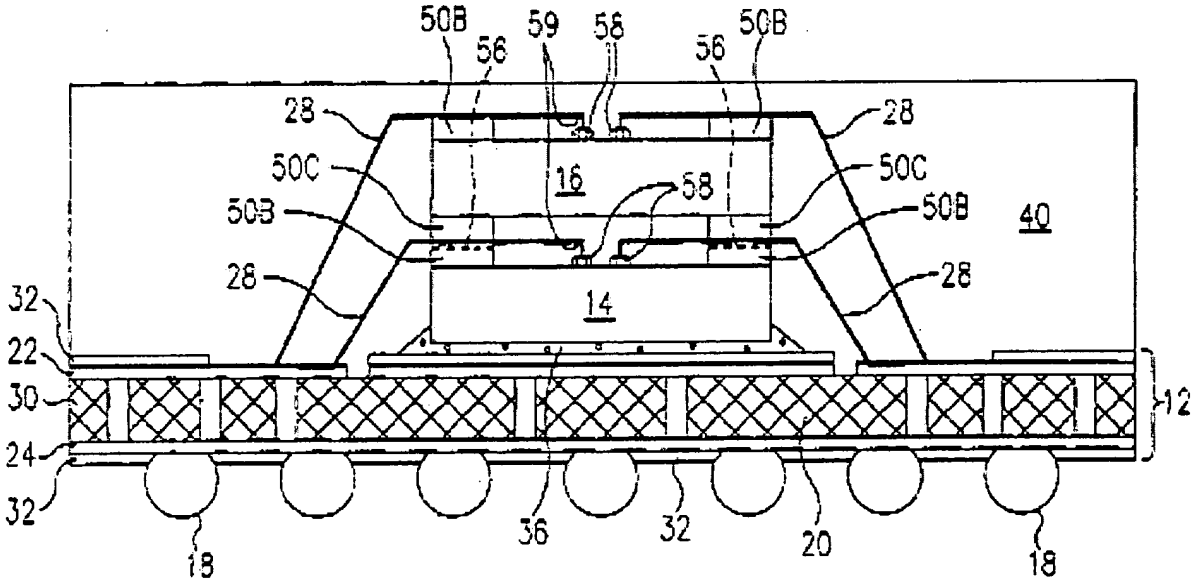
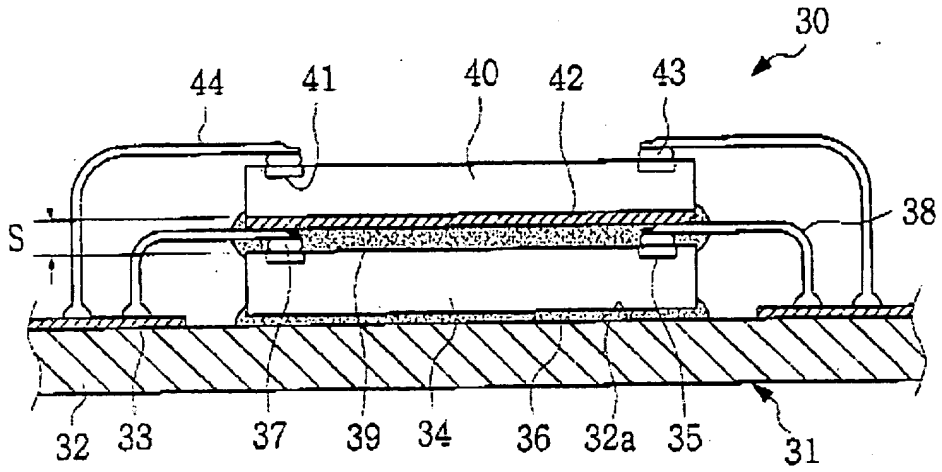


FIG. 9

Shim does not teach that other ends are horizontally attached to the flattened ball. Nevertheless, Kang (e.g. fig. 3) shows electrically conductive wires 38 that run substantially parallel to the surface of the die and have ends that are horizontally

attached to flattened balls 37. According to Kang, this type of connection minimizes a space between the first chip and a second chip, thereby reducing the total height of the semiconductor stack (abstract).



It would have been obvious to one of ordinary skill in the art at the time the invention was made to horizontally attach the other ends of the wires disclosed by Shim to the fattened balls in accordance to Kang's invention to minimize the space between the first and the second chip, thereby reducing the total height of the semiconductor stack.

6. Regarding claim 4, Shim shows that the second substrate contacts are located to accommodate a pin out different from the die.

7. Regarding claim 5, Shim (e.g. fig. 9) shows process for packaging a die comprising the steps of: defining electrical die contacts, the electrical die contacts arranged along a first and an opposite side of the die (i.e. left side from the geometrical center line and right side from the geometrical center line of the chip), defining a substrate 12 with first substrate contacts 22, flattening an electrical conductive balls 58,

attaching the flattened electrically conductive balls to the die contacts, forming electrical conductive runs 22/24 on the substrate 12 that run substantially under the die connecting the first substrate contacts, wherein the first substrate contacts are located adjacent to the first side of the die, to second substrate contacts 22 wherein the second substrate contacts are located adjacent to the opposite side of the die, connecting electrically conductive wires 28 to the first substrate contacts, running the electrically conductive wires substantially parallel to the surface of the die contacts and attaching the other ends of the wires to the flattened electrically conductive balls thereby making electrical connections therebetween and wherein the other ends remain substantially parallel to the surface of the die. Shim does not teach that other ends are horizontally attached to the flattened ball. Nevertheless, Kang (e.g. fig. 3) shows electrically conductive wires 38 that run substantially parallel to the surface of the die and have ends that are horizontally attached to flattened balls 37. According to Kang, this type of connection minimizes a space between the first chip and a second chip, thereby reducing the total height of the semiconductor stack (abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to horizontally attach the other ends of the wires disclosed by Shim to the fattened balls in accordance to Kang's invention to minimize the space between the first and the second chip, thereby reducing the total height of the semiconductor stack.

8. Regarding claim 8, Shim shows that the second substrate contacts are located to accommodate a pin out 18 different from the die.

Response to Arguments

9. Applicant's arguments filed 11/10/2006 have been fully considered but they are not persuasive.

10. Applicant argues that the prior art does not show the new added limitation. However, it is respectfully noted that Shin in view of Kang teaches all limitations. In this case, the limitation "opposite sides" has been interpreted as right and left sides defined by the geometrical center of the chip. As, shown in figure 9 of Shim, the electrical conductive runs on the substrate run substantially under the die connecting first and second substrate contacts which are respectively located at opposite sides of the chip.

11. In response to applicant's argument that Shim does not suggest in any fashion or illustrate in any fashion this left to right reversal to allow the die down die to be placed in a die up package, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Leonardo Andujar
Primary Examiner
Art Unit 2826

08/31/2006